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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,859	12/05/2003	Zhiqing Li	NAY 0001 PA/31558.2	8497
7590 01/23/2006				
DINSMORE & SHOHL LLP Suite 500 One Dayton Centre Dayton, OH 45402-2023			EXAMINER PIZARRO CRESPO, MARCOS D	
			ART UNIT 2814	PAPER NUMBER

DATE MAILED: 01/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/729,859

Applicant(s)

LI ET AL.

Examiner

Marcos D. Pizarro-Crespo

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 May 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-9 and 11-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3-9 and 11-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☒ Claim(s) 1,3-9 and 11-14 are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

Attorney's Docket Number: NAY0001PA/31558.2

Filing Date: 12/5/2003

Claimed Foreign Priority Date: none

Applicant(s): Li et al.

Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the amendment filed on 5/16/2005.

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:
 - I. Claims 1, 3, 4, 9, and 11-14, drawn to a semiconductor device, classified in class 257, subclass 421.
 - II. Claims 5-8, drawn to method of using a semiconductor device, classified in class 324, subclass 200.
2. The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as product and process of using the product. Inventions I and II are distinct if they are disclosed as related, but are capable of separate manufacture, use, or sale as claimed, and are patentable over each other (MPEP § 806.05(f)). In the instant case, unpatentability of the group-I invention would not necessarily imply unpatentability of the group-II invention, since the process of the group-II invention could be applied to a materially different semiconductor device than that of the group-I invention. For example, the step recited in claim 5 of applying an electric field may be performed to a transistor lacking the gate recited in claim 1,

wherein the first and second supplemental gates are differently connected to two different voltage sources instead of the two transistor drains.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. **Applicant is advised that the reply to *this* requirement to be complete must include an election of the invention to be examined** even though the requirement be traversed (37 CFR 1.143).

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Acknowledgment

6. The amendment filed on 5/16/2005, responding to the Office action mailed on 2/16/2005, has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 1, 3-9, and 11-14.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 3, 9,12, and 13 are rejected under 35 U.S.C. 102(a) as being anticipated by Li.

9. Regarding claim 1, Li shows (see, e.g., fig. 2) all aspects of the instant invention including a field effect transistor for detecting a magnetic field comprising:

- ✓ A doped layer
- ✓ Doped source **S** and drain **D** regions formed in the doped layer, the doped layer defining a lengthwise extending channel between the source and drain regions
- ✓ First **D1** and second **D2** drain contacts spaced laterally relative to the length of the channel and located laterally proximate to first and second lateral regions of the channel, respectively, and interconnected with the drain region
- ✓ A gate **G** proximate to the channel for controlling current that may flow from the source and drain region
- ✓ First **FG1** and second **FG2** supplemental gates electrically isolated from each other and the gate and located laterally proximate to the first and second lateral regions, respectively

wherein the first supplemental gate **FG1** is interconnected with the second drain contact **D2**, and the second supplemental gate **FG2** is interconnected with the first drain contact **D1** so that the supplemental gates exert a lateral electric field in the channel as a result of an imbalanced current flow through the first and second drain contacts.

10. Regarding claim 3, Li shows the doped layer is p-type and the source/drain regions are n-type (see, e.g., fig. 2).

11. Regarding claim 9, Li shows (see, e.g., fig. 2) a field effect transistor comprising:

- ✓ A semiconductor substrate
- ✓ A source region **S**
- ✓ A drain region **D**
- ✓ A channel formed in the substrate for guiding current from the source region to the drain region along a lengthwise extent of the channel
- ✓ A gate **G** in proximity to the channel for controlling current from the source to the drain
- ✓ First **D1** and second **D2** drain contacts as part of the drain region for guiding current from a lateral portion of the channel
- ✓ First **FG1** and second **FG2** supplemental gates proximate to the channel for establishing an electric field in the channel in a direction perpendicular to the lengthwise extent

Wherein:

- ✓ the first drain contact **D1** and the first supplemental gate **FG1** are located proximate to a first lateral region of the channel
- ✓ the second drain contact **D2** and the second supplemental gate **FG2** are located proximate to a second lateral region of the channel
- ✓ the first supplemental gate **FG1** is electrically interconnected to the second drain contact **D2**

- ✓ the second supplemental gate **FG2** is electrically interconnected to the first drain contact **D1**

12. Regarding claim 12, Li shows (see, e.g., fig. 2(b)) a magnetic latch wherein the source and the first drain contact are interconnected to an electronic circuit to switch current through the first drain contact to the electronic circuit in the presence of a magnetic field.

13. Regarding claim 13, Li teaches that the magnetic latch may also be used as a magnetic memory element (see, e.g., pp.912/col.2).

14. Claims 1, 9, 11, and 14 rejected under 35 U.S.C. 102(a) as being anticipated by Sun.

15. Regarding claim 1, Sun shows (see, e.g., figs. 1 and 3(a)) all aspects of the instant invention including a field effect transistor for detecting a magnetic field comprising:

- ✓ A doped layer
- ✓ Doped source **S** and drain **D** regions formed in the doped layer, the doped layer defining a lengthwise extending channel between the source and drain regions
- ✓ First **D1** and second **D2** drain contacts spaced laterally relative to the length of the channel and located laterally proximate first and second lateral regions of the channel, respectively, and interconnected to the drain region
- ✓ A gate **G** proximate to the channel for controlling current that may flow from the source and drain region

- ✓ First **FG1** and second **FG2** supplemental gates electrically isolated from each other and the gate and located laterally proximate to the first and second lateral regions, respectively

wherein the first supplemental gate **FG1** is interconnected to the second drain contact **D2**, and the second supplemental gate **FG2** is interconnected to the first drain contact **D1** so that the supplemental gates exert a lateral electric field in the channel as a result of an imbalanced current flow through the first and second drain contacts.

16. Regarding claim 9, Sun shows (see, e.g., figs. 1 and 3(a)) a field effect transistor comprising:

- ✓ A semiconductor substrate
- ✓ A source region **S**
- ✓ A drain region **D**
- ✓ A channel formed in the substrate for guiding current from the source region to the drain region along a lengthwise extent of the channel
- ✓ A gate **G** in proximity with the channel for controlling current from the source to the drain
- ✓ First **D1** and second **D2** drain contacts as part of the drain region for guiding current from a lateral portion of the channel
- ✓ First **FG1** and second **FG2** supplemental gates proximate to the channel for establishing an electric field in the channel in a direction perpendicular to the lengthwise extent

Wherein:

- ✓ the first drain contact **D1** and the first supplemental gate **FG1** are located proximate to a first lateral region of the channel
- ✓ the second drain contact **D2** and the second supplemental gate **FG2** are located proximate to a second lateral region of the channel
- ✓ the first supplemental gate **FG1** is electrically interconnected to the second drain contact **D2**
- ✓ the second supplemental gate **FG2** is electrically interconnected to the first drain contact **D1**

17. Regarding claims 11 and 14, Sun further shows a reset switch Φ connected between the first **FG1** and second **FG2** supplemental gates to reset the latch by shorting the gates (see, e.g., fig. 3(a)).

18. Claims 5-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Bate (US 3714523).

19. Regarding claim 5, Bate shows (see, e.g., figs. 1 and 2) all aspects of the instant invention including a method of detecting a magnetic field in a split drain field effect transistor comprising:

- ✓ a source region **S**
- ✓ a drain region **D**
- ✓ a channel **30** interconnecting the source region to the drain region
- ✓ first **D1** and second **D2** drain contacts for guiding current from laterally spaced portions of the channel

the method comprising applying a controlled electric field, laterally across the channel in a direction parallel to the force experienced by electrons in the channel under the influence of a magnetic field **36** (see, e.g., col.2/ll.30-37).

20. Regarding claim 6, Bate shows the electric field is generated as a result of an imbalanced current flow through the first and second drain contacts (see, e.g., col.2/ll.30-40).

21. Regarding claim 7, Bate shows (see, e.g., figs. 1 and 2) that the electric field is applied to the channel by way of two supplemental gates **G1**, **G2** proximate to the channel.

22. Regarding claim 8, Bate shows a potential difference across the supplemental gates is generated by the imbalanced current flow (see, e.g., col.2/ll.30-45).

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

24. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

25. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Li in view of Bate and Ghandhi.

26. Regarding claim 4, Li shows most aspects of the instant invention (see, e.g., paragraph 9 above), except for p-type source/drain regions formed in an n-type doped layer. Bate (see, e.g., col.1/ll.47-50), on the other hand, teaches that it is understood that the polarities of Li's doped layer and source/drain regions could be advantageously reversed by appropriate modifications well known to those skilled in the art. Ghandhi (see, e.g., pp.731/ll.8-12) further teaches that said modifications would provide a relatively easy to make device.

It would have been obvious at the time of the invention to one of ordinary skill in the art to reverse the polarities of Li's doped layer and source/drain regions to obtain p-type source/drain regions in an n-type layer, as suggested by Bate and Ghandhi, because said modifications would result in a device that is easy to make.

Conclusion

27. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(571) 273-8300**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(571) 272-1716** and between the hours of 9:30 AM to 8:00 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (571) 272-1705.

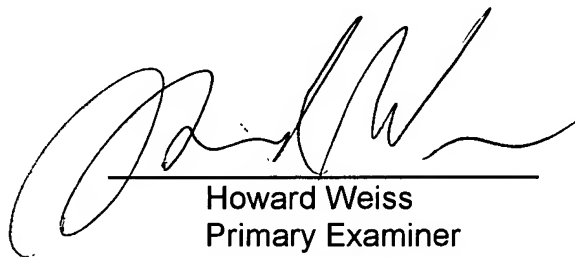
29. Any inquiry of a general nature or relating to the status of this application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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30. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/421-430, 324/200	1/19/2006
Other Documentation:	
Electronic Database(s): EAST (USPAT, EPO, JPO)	1/19/2006

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